ABSTRACT OF THE DISCLOSURE

A configurable coprocessor interface between a central processing unit (CPU) and a coprocessor is provided. The coprocessor interface has an instruction transfer signal group for transferring different instruction types from the CPU to the coprocessor, sequentially or in parallel, a busy signal group, for allowing the coprocessor to signal the CPU that it cannot receive a transfer of one or more of the different instruction types, and an instruction order signal group for indicating to the coprocessor a relative execution order for multiple instructions that are transferred in parallel. In addition, the coprocessor interface includes separate data transfer signal groups for data being transferred from the CPU to the coprocessor, and for data being transferred from the coprocessor to the CPU, along with a data order signal group for indicating a relative order of data (if transferred out-of-order). The interface further includes signal designations which allow for multiple issue groups between the CPU and one or more coprocessors.